Office Action by three months and a Credit Card Payment Form (Form PTO-2038) for payment of the fee for the extension of time ($890) are being filed with this Amendment. Please charge any other fees, if necessary, for entry of this Amendment to our Deposit Account No. 18-1644.

The foregoing amendments to the specification correct informalities noted in a detailed study thereof. Attached hereto is a marked-up version of the changes made to the specification and claims by this Amendment. This marked-up version is entitled "Version With Markings To Show Changes Made."

The Examiner has objected to the Title of the Invention as not descriptive of the invention. Applicant has amended the Title as set forth above, thereby obviating this objection. The amended Title is now believed to appropriately describe the invention.

The Examiner has also objected to the Abstract of the Disclosure as not being in proper language and format. Applicant has requested that the Abstract on file be replaced by the attached Abstract, which is believed to describe the invention in proper language and format.

The Examiner has objected to the drawings because they "fail to show '301' as described in the specification on page 10, line 24." The reference to "301" was in error and applicant has corrected the reference number in the specification to show the correct feature, area 205, thereby obviating the objection.

Claims 1-34 are pending in the application. Independent claims 1, 12, 20 and 29 and dependent claim 18 have been amended.

Claims 1-6, 12-16, 20 and 29-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamagata (U.S. Patent No. 5,764,800) in view of Parulski et al. (U.S. Patent No.

5,633,678). The remaining dependent claims were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamagata in view of Parulski et al. and in further view of Ota (U.S. Patent No. 6,201,571), Honda (U.S. Patent No. 6,181,878), Yonemitsu et al. (U.S. Patent No. 5,510,840) and Jeong (U.S. Patent No. 6,130,988) or some combination thereof. With respect to applicant's claims, as amended, these rejections are respectfully traversed and reconsideration is requested.

Independent claims 1, 12 and 20 have been amended and now recite a signal processing device including the limitations of inputting means for inputting a video signal and memory means having a common memory for storing the video signal to perform a [compressing, expanding or other predetermined process] by said [compressing, expanding or processing] means and storing the character signal generated by said generating means to perform a combining operation of the character signal.

Independent claim 29, directed to a recording apparatus, similarly has been amended to include the above limitations.

It is submitted that the Yamagata and Parulski et al. references, either alone or in combination, do not disclose or suggest the signal processing device as claimed in amended independent claims 1, 12 and 20, or the recording apparatus as claimed in amended independent claim 29.

Particularly, the Yamagata reference does disclose the feature of storing image data picked up by a CCD in the image memory (35) and the structure of a compression/expansion circuit (44) for compressing or expanding the image data. Yamagata also discloses that image data read from the image memory (35) is stored in the IC memory card (M) and that a non-compression mode, a

low compression mode, and a high compression mode can be selected with respect to the image data stored in the IC memory card (M).

As the Examiner pointed out, however, the Yamagata reference fails to teach or suggest generating means for generating a character signal, or that the memory used for image processing, such as compression or expansion of the image signal, is also used for such character signal generation, as claimed in the amended independent claims.

The Parulski et al. reference also does not disclose or suggest the signal processing device or recording apparatus as claimed in the amended independent claims. The Parulski et al. reference does disclose an image buffer (18) storing therein one or more still images, a processor (20) for controlling the image buffer, a date and time generator (20a) which supplies date and time information to the processor (20), a processor (22) for compressing the images using an algorithm such as JPEG, which algorithms are stored in memory (28), and the storage of such compressed image in the memory card (24). However, while the memory card (24) contains additional memory to store header files (24b) for "tagging" the already processed images with character strings, it cannot be said that the device of Parulski et al. uses the same memory for processing (e.g., compressing or expanding) image information as it does for generating character information.

Thus the Parulski et al. reference fails to teach or suggest that the memory used for image processing, such as compression or expansion of the still image, is also used for generating a character signal. Indeed, the Parulski et al. reference teaches a pre-capture use of post-capture image "tagging" that is well known in the art, but it fails to teach or suggest the use of a common memory for both image processing and character generating functions, as claimed in the amended independent claims.

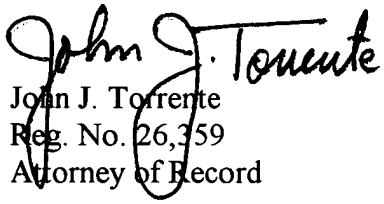
It is therefore submitted that the amended independent claims are patentable based upon the Yamagata and Parulski et al. references, taken alone or together, not disclosing or suggesting the content therein within the meaning of Section 103.

Reliance is placed on In re Fine, 5 U.S.P.Q. 2d 1596, 1600 (Fed. Cir. 1988) and Ex parte Kochan, 131 U.S.P.Q. 204 (Bd. App. 1960) for allowance of the dependent claims, since they differ in scope from the parent independent claims which are submitted as patentable.

Patentability of the claims is believed to have been established. If the Examiner believes that an interview would expedite consideration of this Amendment or of the application, a request is made that the Examiner telephone applicant's counsel at (212) 682-9640.

Dated: November 8, 2001

Respectfully submitted,



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Version With Markings To Show Changes Made

IN THE SPECIFICATION

Page 1, line 2, delete in its entirety and insert:

--SIGNAL PROCESSING DEVICE FOR PROCESSING VIDEO SIGNAL INFORMATION BY USING MEMORY --.

Rewrite the paragraph starting at page at page 10, line 15 and ending at page 10, line 26, as follows: -- As shown in Fig. 2, in the VTR according to the embodiment, there is provided the memory 125 which is commonly accessed by each of the input/output processing circuits, the compression/expansion circuits, the error correction processing circuits, and recording/reproduction processing circuits, and addresses of the memory are differently allotted to the respective circuits depending on the usage thereof. The superimposition data generating circuit 123 generates superimposition data by using the area [301] 205 other than areas which are accessed by the recording/reproduction-system circuits in the memory 125. --.

Rewrite the paragraph starting at page at page 13, line 3 and ending at page 13, line 9, as follows: -- The combining circuit 217 combines the video signal inputted from the terminal 213 and the character signal for display outputted from the table memory [217] 211, in accordance with the operation control signal outputted from the table memory 211, and outputs the thus-obtained composite signal to an RGB conversion circuit 221 and a selector 225. --.

Rewrite the paragraph starting at page at page 13, line 17 and ending at page 13, line 20, as follows:

-- The RGB conversion circuit [211] 221 converts the composite video signal outputted from the combining circuit 217 into RGB signals and outputs the RGB signals to the EVF 301. --.

IN THE CLAIMS

Amend claims 1, 12, 18, 20 and 29 as follows:

-- 1. (Amended) A signal processing device [for processing a signal by using a memory], comprising:

inputting means for inputting a video signal;

compressing means for compressing an amount of information of [a] the video signal [by using said memory]; [and]

generating means for generating a character signal [by using said memory]; and

memory means having a common memory for storing the video signal to perform a compressing process by said compressing means and storing the character signal generated by said generating means to perform a combining operation of the character signal. --.

-- 12. (Amended) A signal processing device [for processing a signal by using a memory], comprising:

inputting means for inputting a video signal;

expanding means for expanding an amount of information of [a] the video signal [by using said memory]; [and]

generating means for generating a character signal [by using said memory]; and

memory means having a common memory for storing the video signal to perform an expanding process by said expanding means and storing the character signal generated by said generating means to perform a combining operation of the character signal. --.

-- 18. (Amended) A device according to claim 12, wherein said memory has a first area which is to be accessed by said [compressing] expanding means, and a second area which corresponds to an image plane represented by the video signal and which is different from said first area, and wherein said generating means comprises memory control means for writing into said second area a plurality of codes representing a value of pixel data of the character signal, and a table for outputting pixel data corresponding to codes read out from said second area. --.

-- 20. (Amended) A signal processing device [for processing a signal by using a memory], comprising:

inputting means for inputting a video signal;

processing means for [processing a] performing a predetermined process on the video signal [by using said memory]; [and]

generating means for generating a character signal [by using said memory]; and

memory means having a common memory for storing the video signal to perform the predetermined process by said processing means and storing the character signal generated by said generating means to perform a combining operation of the character signal. --.

-- 29. (Amended) A recording apparatus, comprising:

[a memory;]

inputting means for inputting a video signal;

compressing means for compressing an amount of information of [a] the video signal [by using said memory];

recording means for recording on a recording medium the video signal the amount of which has been compressed by said compressing means; [and]

generating means for generating a character signal [by using said memory]; and

memory means having a common memory for storing the video signal to perform a compressing process by said compressing means and storing the character signal generated by said generating means to perform a combining operation of the character signal. --.

ABSTRACT OF THE DISCLOSURE

A signal processing device having a video signal input, a circuit for processing a video signal, a generating device for generating a character signal, and a memory for storing the video signal to be processed and for storing the character signal generated by the generating device. The processing circuit may include a high-efficiency encoding unit for compressing information of the video signal and encoding the video signal, or a high-efficiency decoding unit for decoding the video signal and expanding the decoded video signal, and the memory has a first area to be accessed by the encoding unit or by the decoding unit and a second area used by the generating device to generate the character signal.